

Design and Performance of Wideband GaAs MMIC's for High-Speed Optical Communication Systems

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Abstract—Advanced design techniques for GaAs wideband direct-coupled amplifiers are described. The amplifier achieved a 20-dB gain with a 3-dB bandwidth of 13 GHz and 5–7-dB noise figure. An equalizing amplifier module consisting of amplifier and variable attenuator MMIC's exhibited a high gain of 43 dB over a 10-GHz band with a controllable gain of 20–43 dB.

I. INTRODUCTION

HIGH-GAIN and wideband MMIC modules operating from dc to over 10 GHz are required for very high-speed optical communication systems. A direct-coupled amplifier IC is essential to realize the module because it provides a high gain from dc and has a small chip size compared with other circuits. A number of direct-coupled amplifiers have been developed using GaAs MESFET's and heterostructure devices [1], [2]. GaAs amplifiers are more realistic candidates to realize the systems considering the maturity of the device technology. A key design issue is to maximize the bandwidth of the amplifier while maintaining a low VSWR and low noise figure with the relatively limited MESFET performance. This paper describes several innovative design techniques for GaAs direct-coupled amplifiers and an application to an equalizing amplifier module. A key feature of the design is to employ a cascode FET with multiple feedback and a matching network to realize wide bandwidth and good impedance matching characteristics. A voltage-controlled variable attenuator MMIC was also developed for gain-control use in an equalizing amplifier module.

II. CIRCUIT DESIGN

Circuit simulation was performed using an FET model with an f_t of 40 GHz and an f_{max} of 70 GHz.

A. Direct-Coupled Amplifier

First we discuss the basic configuration of an amplifier and then describe the complete configuration.

Basic Amplifier (Amplifier I): Fig. 1 shows a schematic of amplifier I (Circuit A). The amplifier implements output source-followers which are connected to the drain terminal of the input FET. This arrangement provides an

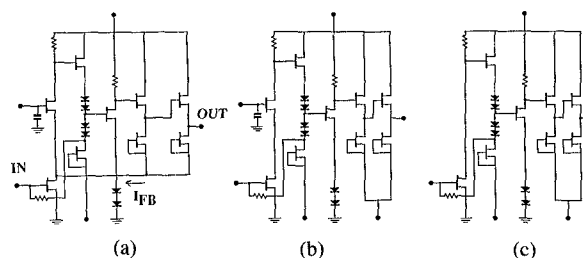


Fig. 1. Schematics of direct-coupled amplifiers. (a) Amplifier I. (b) Cascode amplifier. (c) Basic feedback amplifier.

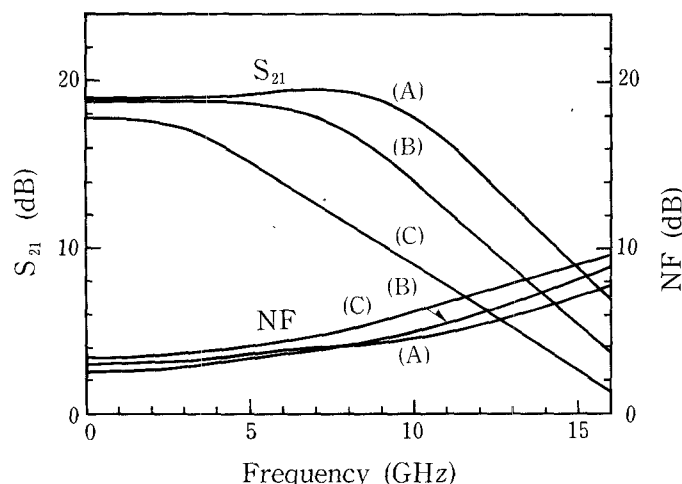


Fig. 2. Simulated frequency characteristics. (a) Amplifier I. (b) Cascode amplifier. (c) Basic feedback amplifier.

additional feedback loop through the source-followers. The performance of the amplifier was compared with conventional circuits B and C, and the simulated performance is shown in Fig. 2. The cascode FET amplifier (Circuit B) had about 3 GHz wider bandwidth than the feedback amplifier (Circuit C) because of the reduced Miller effect. Amplifier I had about 3 GHz wider bandwidth than the cascode FET amplifier. As a result, it provided about twice the bandwidth of the conventional feedback amplifier. This improvement was achieved by designing the negative feedback to become positive at high frequency using the extra phase delay of the cascode FET [3]–[5]. Fig. 3 shows a vector diagram of the normalized feedback current. The vector diagram shows that the negative feedback becomes positive with increasing frequency. The feedback current had a 180 out-of-phase component above 9 GHz with respect to its phase at low frequency. The

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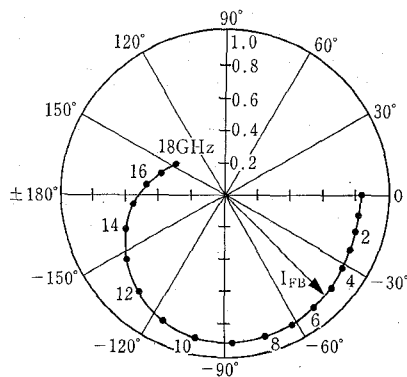


Fig. 3. Vector diagram of feedback current.

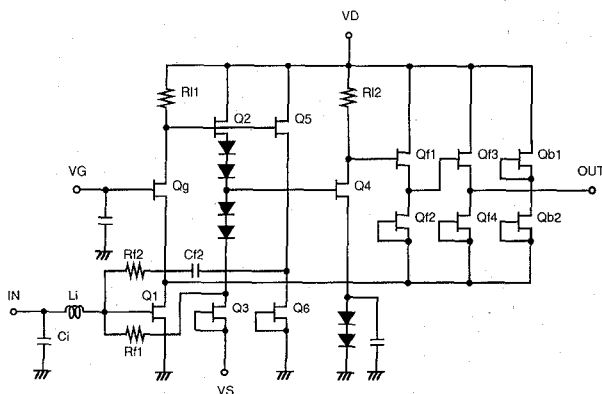
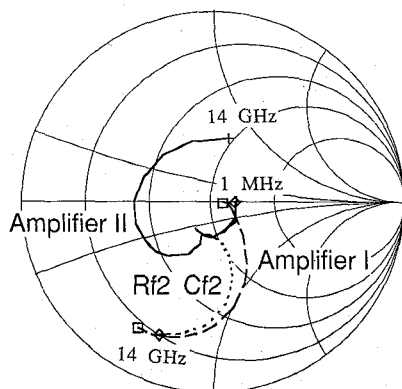


Fig. 4. Schematic of amplifier II.

Fig. 5. Impedance mapping of S_{11} (1MHz-14GHz). —: Amplifier II. -----: Amplifier I with R_{f2} and C_{f2} . -.-: Amplifier I.

frequency at which positive feedback starts is optimized by selecting the gate width of the common-gate FET. The degree of feedback is controlled by the gate widths of source-followers.

Complete Amplifier (Amplifier II): Fig. 4 shows a schematic of amplifier II which is a modified version of amplifier I. The amplifier employs an additional feedback loop and matching network to improve the input matching over a wide frequency band. The feedback loop consists of source-follower, resistor R_{f2} and capacitor C_{f2} . The matching network consists of inductor L_i and capacitor C_i . S_{11} is plotted from 1 MHz to 14 GHz on a Smith Chart as shown in Fig. 5. The loci of S_{11} clearly shows

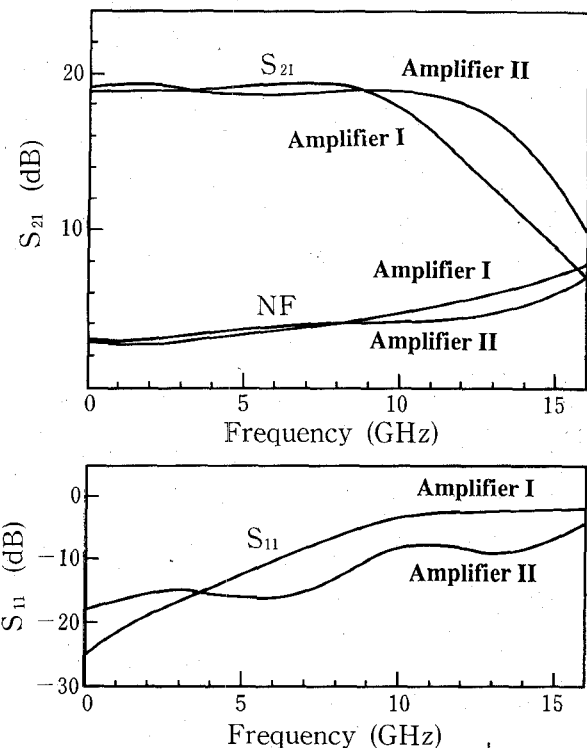


Fig. 6. Simulated frequency characteristics of amplifiers I and II.

the effect of the additional circuits on input matching. In amplifier I, the real part of the input admittance decreased with increasing frequency due to the extra phase delay of the cascode FET. This admittance decrease affected S_{11} . RC feedback compensated for this effect thus reducing S_{11} . At high frequency, S_{11} was still large since it was affected by the input capacitive component. The matching network canceled the component and reduced S_{11} at high frequency. Fig. 6 shows the simulated performance of amplifier II. It maintained good input matching over a 10-GHz frequency band. A noise figure at high frequencies was also reduced compared with amplifier I because a high-frequency gain response of the first stage (FETQ1) was improved. The stability factor was also evaluated during the design and it kept greater than unity from dc to 20 GHz.

B. Variable Attenuator

An equalizing module required a gain-control amplifier. To maintain wide bandwidth and good gain flatness at various gain states in a gain-control amplifier is very difficult because signals usually bypass the main pass at high frequencies through the parasitic capacitances. Also, since the gain is usually reduced by advancing the gate voltage toward pinch-off in most gain-control amplifiers, the output waveform is distorted at low-gain states. To overcome these problems, a voltage-controlled variable attenuator was employed for gain-control use in an equalizing amplifier module. The variable attenuator uses FET's as variable resistors and has demonstrated wide bandwidth and good linearity [6]. A schematic of the

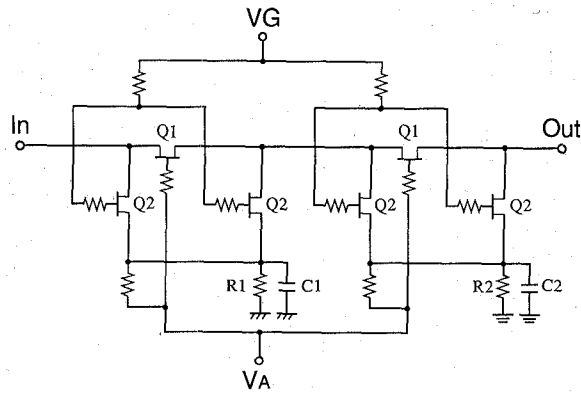


Fig. 7. Schematic of variable attenuator.

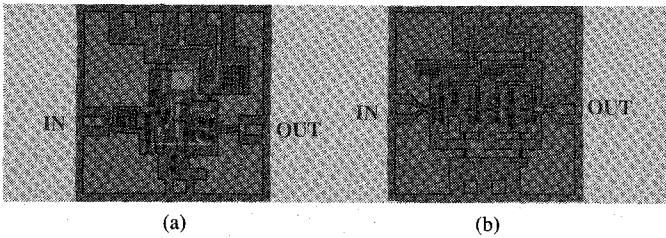


Fig. 8. Microphotograph of MMIC's. (a) Amplifier. (b) Variable attenuator.

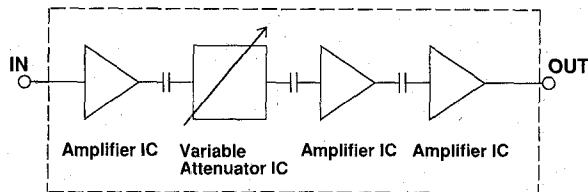


Fig. 9. Block diagram of equalizing amplifier module.

variable attenuator is shown in Fig. 7. In this configuration, attenuation is primarily set by the impedance of the series FET ($Q1$) while the impedance of the shunt FET's ($Q2$) are optimized to maintain a good impedance matching. The attenuation was controlled by a single bias voltage using the self-bias circuitry to simplify the power supply requirement. In the self-bias attenuator, the maximum attenuation was limited at a low frequency due to the biasing resistors at the sources of FET's. This is obviously undesirable for a variable attenuator operating from dc frequency. To get around this problem, two variable attenuators were direct-coupled to increase the maximum attenuation. S_{21} , S_{11} and S_{22} at high frequencies were improved by optimizing the by-pass capacitors ($C1$ and $C2$) parallel to the biasing resistors ($R1$ and $R2$). Circuit simulation leads us to expect a 4-dB insertion loss and 20-dB dynamic range of attenuation from dc to 20 GHz.

III. FABRICATION

MMIC's were fabricated using an advanced self-aligned implantation for n^+ layer technology (ASAINT) [7]. ft and max of MESFET's were 40 GHz and 70 GHz, respectively. Amplifier II was fabricated for the wideband

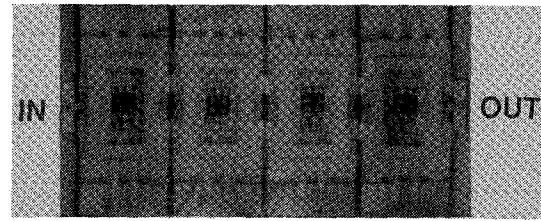


Fig. 10. Microphotograph of module.

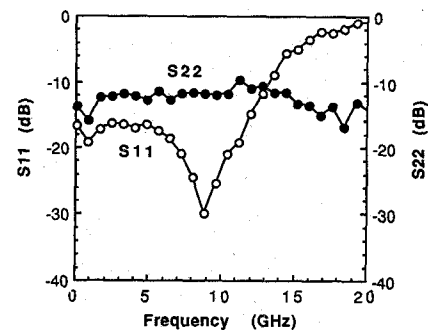
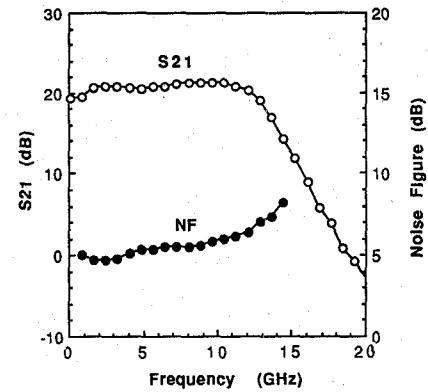


Fig. 11. Frequency characteristics of amplifier.

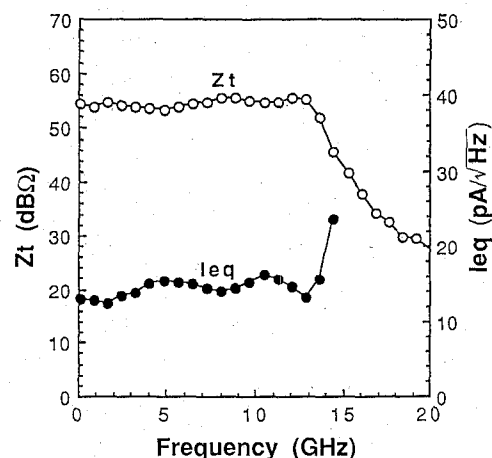


Fig. 12. Frequency characteristics of transimpedance and equivalent input noise current of amplifier.

amplifier, because of the anticipated high performance. Microphotographs of the MMIC's are shown in Fig. 8. The amplifier and variable attenuator chips were both 1.5×1.5 mm.

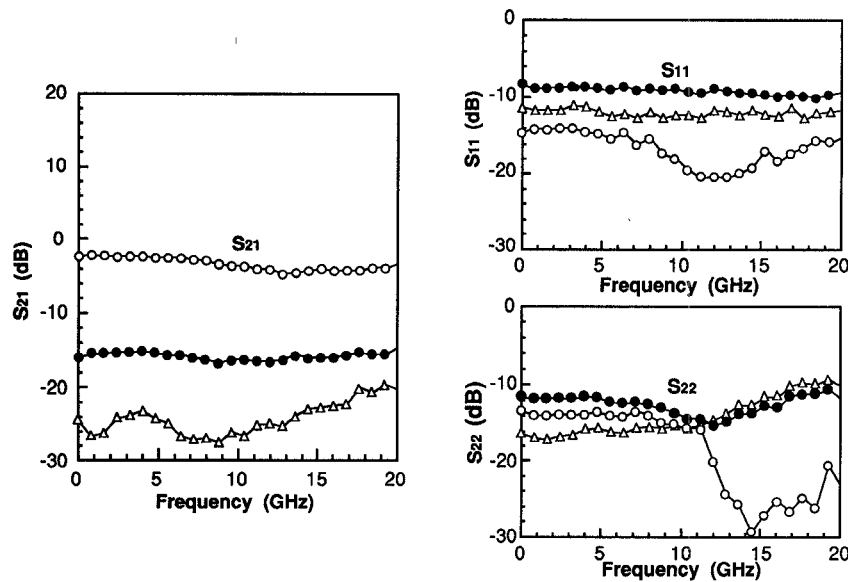


Fig. 13. Frequency characteristics of variable attenuator. ○: VA = 0 V. ●: VA = 1.65 V. △: VA = 1.85 V.

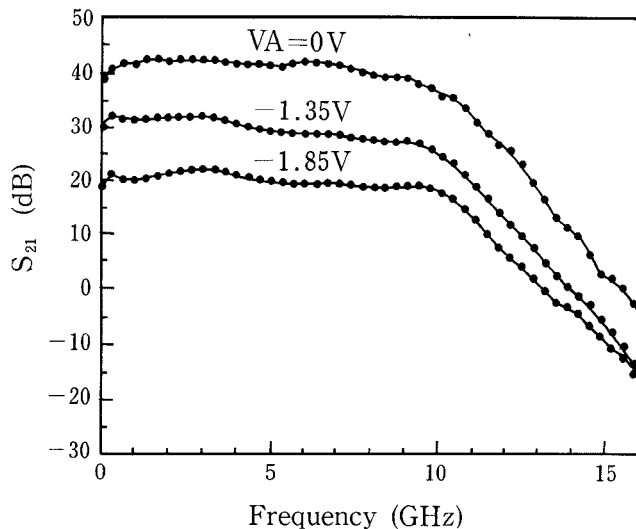


Fig. 14. Frequency dependency of gain for a module at various gain states.

A block diagram of the equalizing amplifier module is shown in Fig. 9. It was fabricated using three packaged amplifiers, one packaged variable attenuator and chip capacitors for dc blocks. A microphotograph of the module is shown in Fig. 10. A single-chip metal package with built-in damping resistors for biasing lines was specially designed to prevent gain ripples at low frequencies [8].

IV. PERFORMANCE

A. Direct-Coupled Amplifier

The performance of amplifier II is shown in Fig. 11. The amplifier had a gain of 20 dB with a 3-dB bandwidth of 13 GHz. It had a noise figure of 5–7 dB over the 13-GHz band. S_{11} and S_{22} were less than -10 dB within the 13-GHz band. To our knowledge, this is the widest bandwidth at a high gain of 20 dB that has been reported for state-of-the-art direct-coupled amplifiers using GaAs

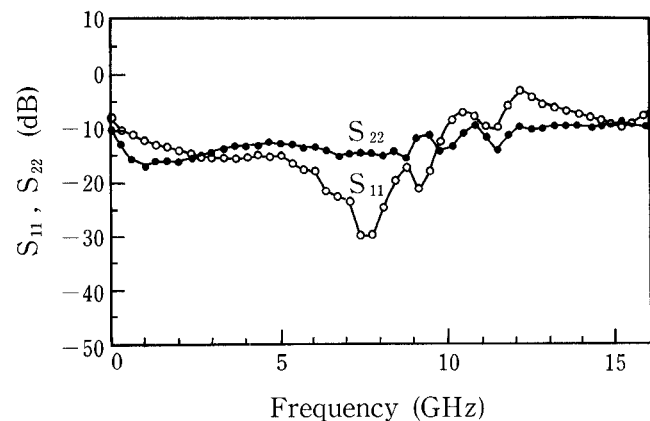


Fig. 15. Frequency dependencies of S_{11} and S_{22} for a module.

MESFET's. Transimpedance and equivalent input noise current were calculated using the measured S parameter and NF to evaluate the performance for the preamplifier as an optical receiver. The detector capacitance and bonding-wire inductance were assumed to be 0.2 pF and 0.3 nH. Results are shown in Fig. 12. The amplifier had a 3-dB bandwidth of 13 GHz with a noise current of less than $15 \text{ pA}/\sqrt{\text{Hz}}$. This indicates that the amplifier can be applied to high-speed and low-noise preamplifiers for optical receivers.

B. Variable Attenuator

Frequency dependencies of S_{21} , S_{11} and S_{22} at various control voltages are shown in Fig. 13. Insertion loss, and reflection coefficient were 2–4 dB, and below -8 dB, respectively, in a 15-GHz frequency band. The dynamic range of attenuation was about 20 dB in a 15-GHz frequency band. The changes of S_{11} and S_{22} above 10 GHz were probably caused by the by-pass capacitors (C_1 and C_2).

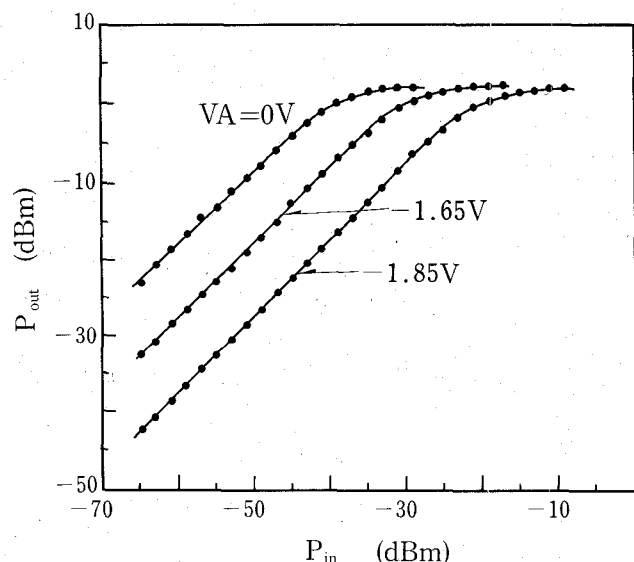


Fig. 16. Output power versus input power for a module at various gain states.

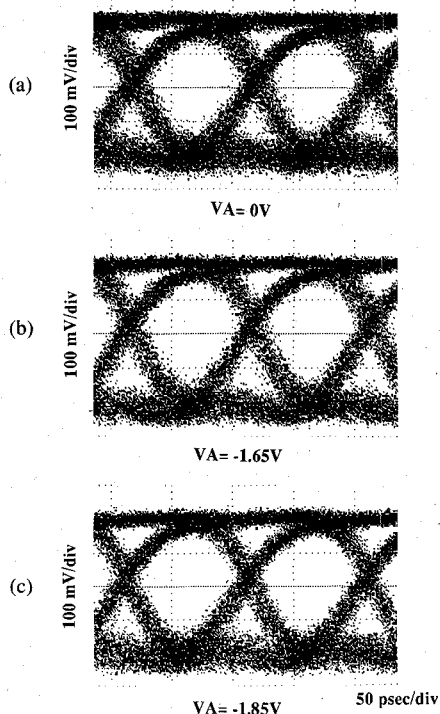


Fig. 17. 10-Gb/s eye patterns at module output. (a) Maximum gain. (b) 10-dB gain reduction. (c) 20-dB gain reduction.

C. Equalizing Amplifier

Gain performance of the module is shown in Fig. 14. It exhibited a high gain of 43 dB with a 3-dB bandwidth of 10 GHz. The gain was controlled from 20 dB to 43 dB using the single bias of the variable attenuator MMIC. Frequency dependencies of S_{11} and S_{22} are shown in Fig. 15. S_{11} and S_{22} were less than -8 dB and 10-GHz frequency band. They were not changed during the gain control. A plot of the output power versus input power at various gain states are shown in Fig. 16. The saturation

power was about 2 dBm. The gain was uniformly controlled at a 20-dB input power range. The output eye patterns at various gain states for 10 Gb/s NRZ $2^{23}-1$ pseudorandom bit stream (PRBS) are shown in Fig. 17. Fairly good eye openings were obtained. They were not influenced by the gain control. These results demonstrate that the developed module can be applied to very-high-speed optical communication systems.

V. CONCLUSION

GaAs wideband direct-coupled amplifiers and equalizing amplifier module with over 10-GHz bandwidth were developed. Given their wide bandwidth, high gain and small size, these devices should make quite an impact on high-speed optical communication systems.

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REFERENCES

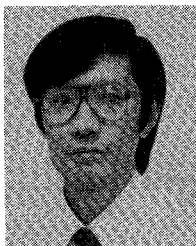
- [1] H. Yamakawa, H. Ibe, J. Akagi, Y. Kuriyama, K. Morizuka, and M. Obara, "10 Gbit/sec HBT preamplifier IC for lightwave transmission," in *Proc. European Conference on Optical Communication*, 1989, pp. 340-342.
- [2] K. Miyagawa, Y. Miyamoto, and K. Hagimoto, "7 GHz bandwidth optical front-end circuit using GaAs FET," *Electron Lett.*, vol. 25, pp. 1305-1306, Sept. 1989.
- [3] K. Osafune, N. Kato, T. Sugeta, and Y. Yamao, "A low-noise GaAs monolithic broad-band amplifier using a drain current saving technique," *IEEE Trans., Microwave Theory Tech.*, vol. MTT-33, pp. 543-545, 1985.
- [4] Y. Imai, M. Tokumitsu, K. Onodera, and K. Asai, "10 GHz bandwidth, 20 dB gain low-noise direct-coupled amplifier ICs using Au/WSiN GaAs MESFET," *Electron Lett.*, vol. 26, pp. 699-700, May 1990.
- [5] W. T. Collieran, and Asad A. Abidi, "A 3.2 GHz, 26 dB wide-band monolithic matched GaAs MESFET feedback amplifier using cascode," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1377-1385, Oct. 1988.
- [6] Y. Tajima, T. Tsukii, R. Mozzi, E. Tong, L. Hanes, and B. Wrona, "GaAs monolithic wideband (2-18 GHz) variable attenuators," in *1982 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 479-481.
- [7] Y. Yamane, M. Ohhata, H. Kikuchi, K. Asai, and Y. Imai, "A 0.2 μ m GaAs MESFET Technology for 10 Gbit/s Digital and Analog IC's," to be published in *1991 MTT-S Int. Microwave Symp. Dig.*
- [8] E. Sano, N. Ishihara, Y. Imai, H. Kikuchi, and Y. Yamane, "A 10Gb/s GaAs MESFET equalizer IC module," to be published in *1991 IEEE VLSI Symp. Dig.*, pp. 79-80.



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